**Phase 2 report**

**Alu**

Input:

|  |  |  |  |
| --- | --- | --- | --- |
| Signal | Direction | Width | Description |
| A | in | 16-bit | First operand (from register Rs) |
| B | in | 16-bit | Second operand (from register Rt or immediate) |
| ALUctr | in | 4-bit | Selects operation type |
| shamt | in | 3-bit | Shift amount (0–7) |
| Result | out | 16-bit | Operation result |
| Zero | out | 1-bit | High if Result = 0 |
| Overflow | out | 1-bit | High if arithmetic overflow occurred |
| Carryout | out | 1-bit | High if carry out from MSB |

**Register file**

input/output

|  |  |  |  |
| --- | --- | --- | --- |
| Signal | Direction | Width | Description |
| clk | in | 1-bit | Clock signal |
| rst | in | 1-bit | Reset (active high) |
| RegWr | in | 1-bit | Write enable |
| Rw | in | 3-bit | Destination register address |
| Ra | in | 3-bit | Source register 1 address |
| Rb | in | 3-bit | Source register 2 address |
| busW | in | 16-bit | Data to write to Rw |
| busA | out | 16-bit | Data from Ra |
| busB | out | 16-bit | Data from Rb |

Initial values

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Address (Binary) | Register Symbol | name | Initial Value (Hex) | Purpose / Description |
| 000 | $r0 | $v0 | 0x0040 | Result register |
| 001 | $r1 | $v1 | 0x1010 | General-purpose register |
| 010 | $r2 | $v2 | 0x000F | General-purpose register |
| 011 | $r3 | $v3 | 0x00F0 | General-purpose register |
| 100 | $r4 | $t0 | 0x0000 | Temporary register |
| 101 | $r5 | $a0 | 0x0010 | Address register |
| 110 | $r6 | $a1 | 0x0005 | Loop counter |
| 111 | $r7 | — | 0x0000 | Reserved |

**16-bit Adder**

Input/output

|  |  |  |  |
| --- | --- | --- | --- |
| Signal | Direction | Width | Description |
| A | in | 16-bit | First operand |
| B | in | 16-bit | Second operand |
| Cin | in | 1-bit | Carry input |
| Sum | out | 16-bit | A + B + Cin |
| Cout | out | 1-bit | Carry output |

**Alu Control**

Input/output

|  |  |  |  |
| --- | --- | --- | --- |
| Signal | Direction | Width | Description |
| opcode | in | 4-bit | Instruction opcode [15:12] |
| ALU\_OP | in | 2-bit | ALU operation type (from Control Unit) |
| ALUctr | out | 4-bit | ALU operation code (to ALU) |

**Control unit**

Input/output

|  |  |  |  |
| --- | --- | --- | --- |
| Signal | Direction | Width | Description |
| opcode | in | 4-bit | Instruction opcode [15:12] |
| reg\_dst | out | 1-bit | 0=Rt, 1=Rd |
| jump | out | 1-bit | Jump enable |
| branch | out | 1-bit | Branch enable |
| mem\_read | out | 1-bit | Memory read enable |
| mem\_to\_reg | out | 1-bit | Write memory data to register |
| ALU\_OP | out | 2-bit | ALU operation control |
| mem\_write | out | 1-bit | Memory write enable |
| alu\_src | out | 1-bit | ALU B source (0=register, 1=immediate) |
| reg\_write | out | 1-bit | Register write enable |